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(54) Image decoding apparatus having frame rate transformation function

(57) An image decoding apparatus having a frame rate transform function includes a first frame rate generator (50) generating a frame rate of a received coded image signal, a second frame rate generator (60) generating a frame rate of an image display device, and a frame rate transformer (70) generating an omission control signal for omitting a predetermined frame when the frame rate of the input image signal is larger than the frame rate of the image display device, while generating a repetition control signal for repeating a predetermined frame when the frame rate of the image signal is smaller than the frame rate of the image display device, and outputting the generated control signal to a decoder (20).

FIG. 2

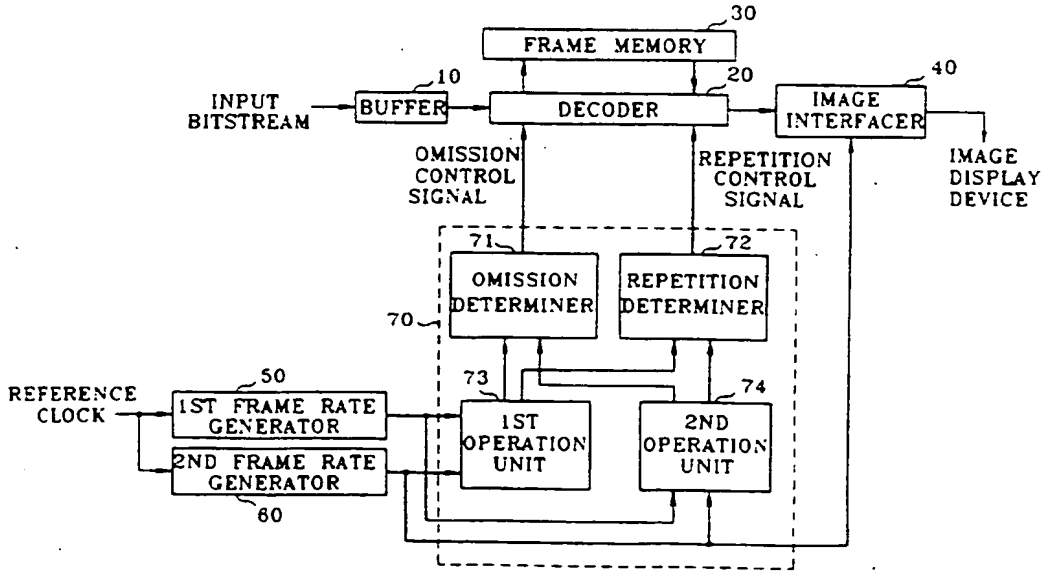

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FIG. 1

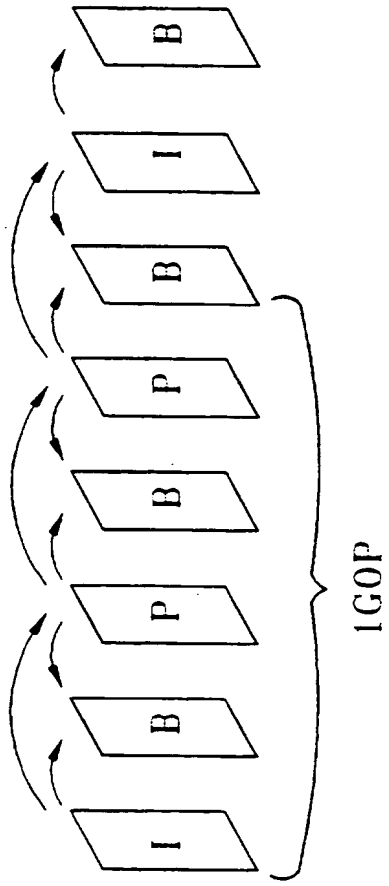

FIG. 2

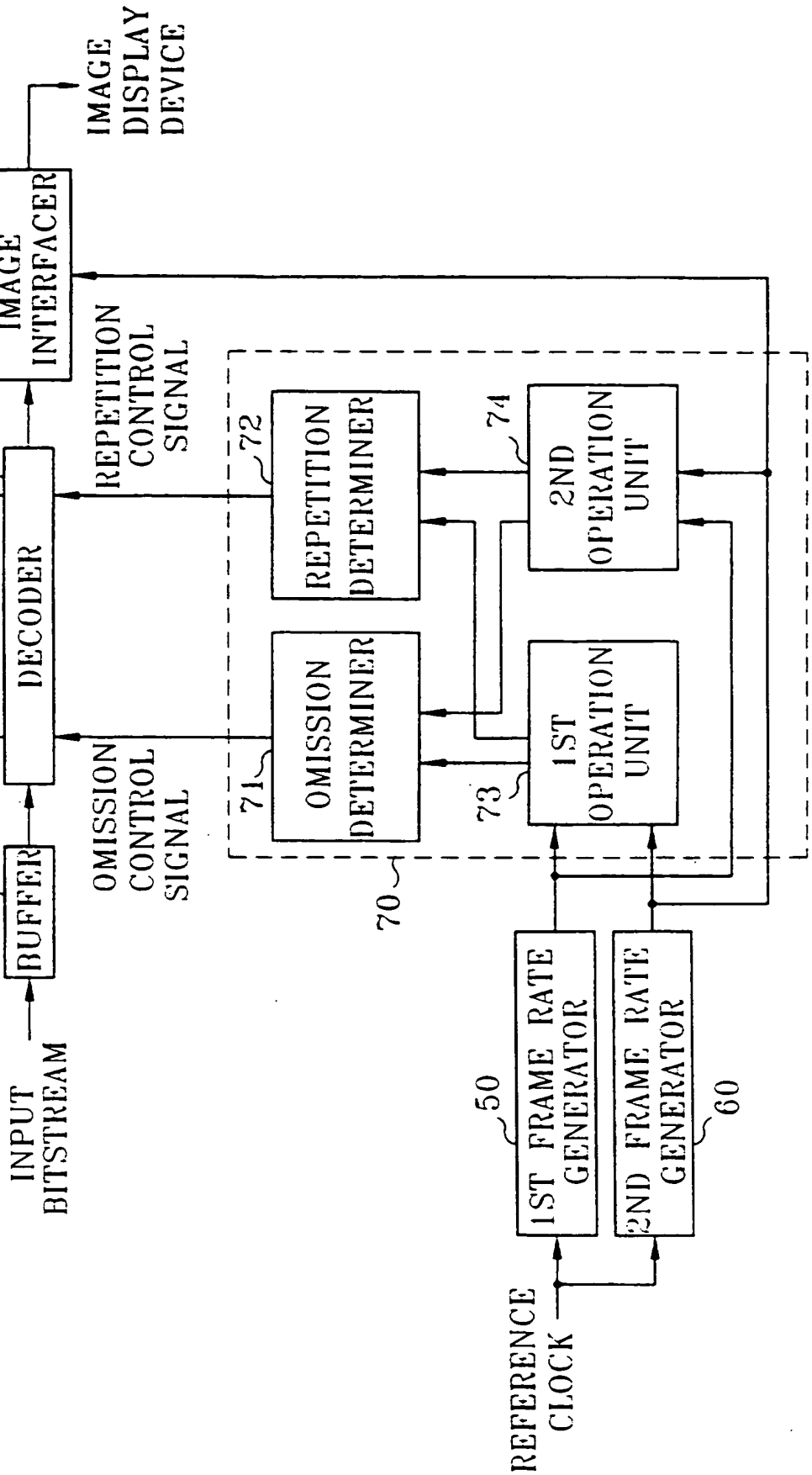
IMAGE DISPLAY DEVICE
40
IMAGE INTERFACER
30
FRAME MEMORY
20
DECODER
10
BUFFER
INPUT BITSTREAM
REPETITION CONTROL SIGNAL
OMISSION CONTROL SIGNAL
72
REPETITION DETERMINER
71
OMISSION DETERMINER
74
2ND OPERATION UNIT
73
1ST OPERATION UNIT
70
50
1ST FRAME RATE GENERATOR
60
2ND FRAME RATE GENERATOR
REFERENCE CLOCK

FIG. 3A

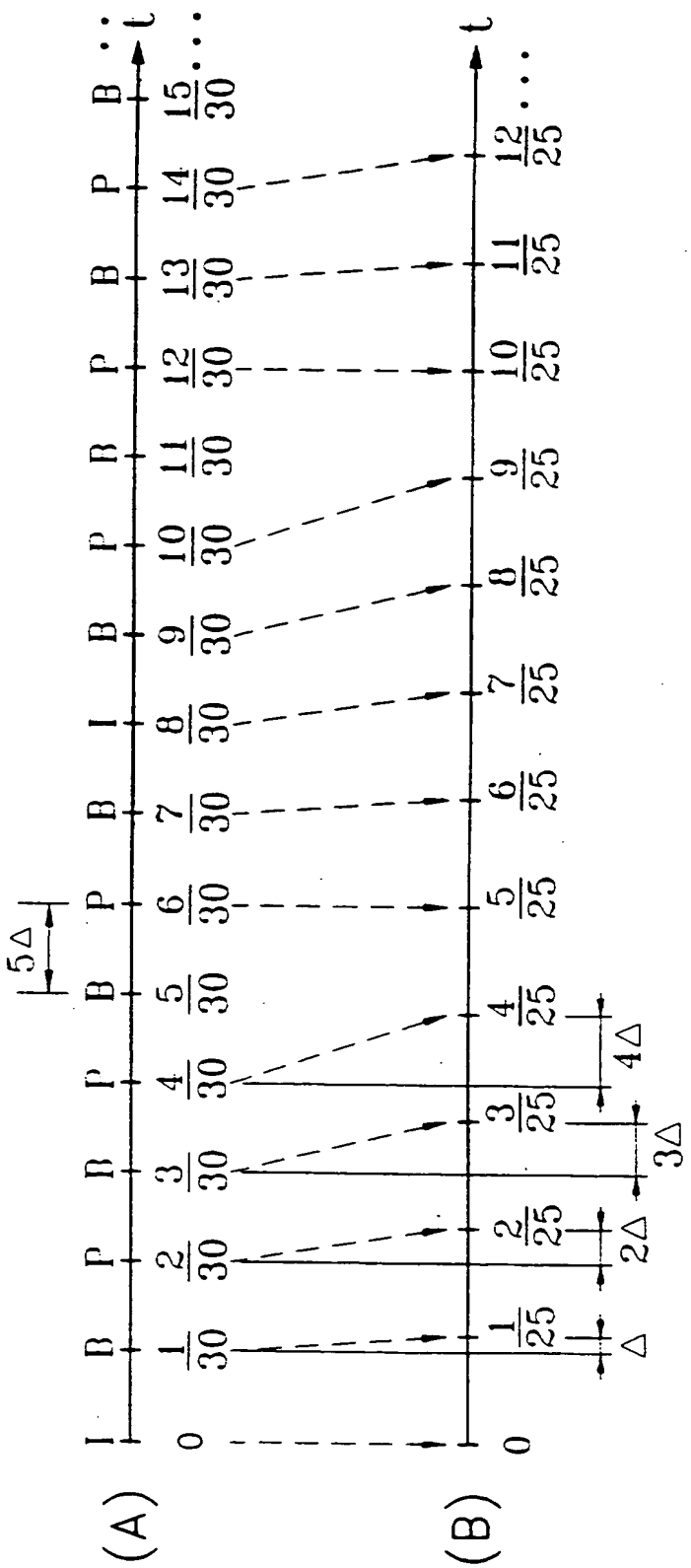
(A)
(B)
t
I B P B P B I B P B P B P B ...
0 1/30 2/30 3/30 4/30 5/30 6/30 7/30 8/30 9/30 10/30 11/30 12/30 13/30 14/30 15/30 ...
0 1/25 2/25 3/25 4/25 5/25 6/25 7/25 8/25 9/25 10/25 11/25 12/25 ...
5Δ
Δ
2Δ
3Δ
4Δ

FIG. 3B

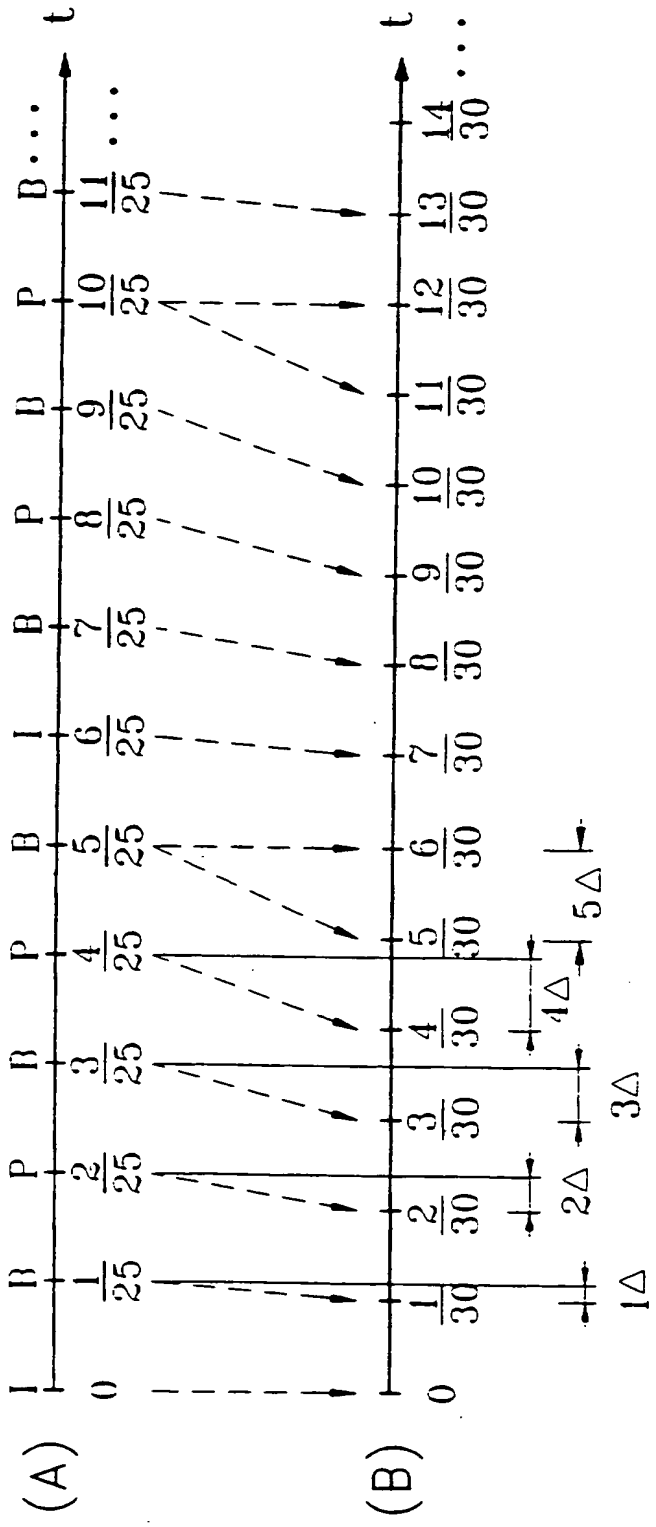
(A)
(B)
t
I B P B P B I B P B P B ...
0 1/25 2/25 3/25 4/25 5/25 6/25 7/25 8/25 9/25 10/25 11/25 ...
0 1/30 2/30 3/30 4/30 5/30 6/30 7/30 8/30 9/30 10/30 11/30 12/30 13/30 14/30 ...
1Δ
2Δ
3Δ
4Δ
5Δ

IMAGE DECODING APPARATUS HAVING FRAME RATE TRANSFORMATION FUNCTION

The present invention relates to an image decoding apparatus, and more particularly, though not exclusively, to an image decoding apparatus having a frame rate transformation function in which an input image signal having a frame rate different from that of an image display device is transformed to have the frame rate of the image display device and the transformed image signal is output.

In recent satellite broadcasting, the satellite broadcast to one country propagates into neighbouring countries, and vice versa. Thus, it is expected that viewers would frequently view the satellite broadcastings from neighbouring countries, according to the various desires of viewers.

However, since a TV receiver of each country is manufactured on the basis of its own TV broadcasting mode, only an image which has the same broadcasting mode as that of the country can be displayed on a screen. That is, an image signal which propagates according to a different broadcasting mode cannot be viewed using the current TV receiver. To enable viewers to view the satellite broadcasting, a broadcasting station should transform a frame rate of an image signal using an expensive transformation apparatus and re-record the transformed image signal, to then transmit it to the TV receivers of each home. In this case, only a broadcasting program frame rate of which has been transformed can be viewed. As a result, the viewers cannot freely view desired programs.

Therefore, viewers need a TV receiver which can receive and display images more freely irrespective of a broadcasting mode. Such a need will be enlarged in a high-definition TV broadcasting.

It is an aim of preferred embodiments of the present invention to provide an image decoding apparatus having a frame rate transformation function which can transform a compressively coded input bitstream into a frame rate of an image display device and output the transformed bitstream, when a frame rate of the compressively coded input bitstream differs from that of the image display device.

According to the present invention in a first aspect, there is provided an image decoding apparatus which transforms a coded image signal having a frame rate different from that of an image display device to have the frame rate of the image display apparatus and outputs the transformed image signal, the image decoding apparatus comprising :

decoding means for decoding the received coded image signal;

first frame rate generation means for generating a first frame rate of the coded image signal based on a predetermined reference clock signal;

second frame rate generation means for generating a second frame rate of an image display device based on the reference clock signal;

frame rate transformation means for receiving the first and second frame rates respectively generated from the first and second frame rate generation means, and generating an omission control signal for omitting a predetermined frame when the first frame rate is larger than the second frame rate, while generating a repetition control signal for repeating a predetermined frame when the first frame rate is smaller than the second frame rate; and

image interfacing means for outputting a frame sequence output from said decoding means to meet the frame rate of said image display device.

Suitably, said frame rate transformation means generates an omission or repetition control signal based on a delay time for outputting a predetermined frame of the input bitstream to have the frame rate of said image display device.

Suitably, said frame rate transformation means generates an omission control signal when said delay time is not less than a predetermined threshold value.

Suitably, said frame rate transformation means generates an omission control signal when said delay time is not less than the predetermined threshold value and the corresponding frame is a bidirectionally-coded (B) frame.

Suitably, said frame rate transformation means generates a repetition control signal when a sign of said delay time is negative and an absolute value of said delay time is not less than a predetermined threshold value.

Suitably, said threshold value is set to be somewhat smaller than the frame rate of the input bitstream.

Suitably, said threshold value is set to be somewhat smaller than the frame rate of the input bitstream.

Suitably, said frame rate transformation means comprises :

a first operation unit for calculating a predetermined threshold value;

a second operation unit for calculating a time delayed for outputting the input signal to have the frame rate of said image display device;

an omission determiner for receiving the threshold value and the delay time and generating an omission control signal when a sign of the delay time is positive and an absolute value thereof is larger than the threshold value; and

a repetition determiner for receiving the threshold value and the delay time and generating a repetition control signal when a sign of the delay time is negative and an absolute value is larger than the threshold value.

According to the present invention in a second aspect, there is provided an image decoding apparatus for transforming a coded image signal having a first frame rate to a signal suitable for display on an image display apparatus operating at a second frame rate, the image decoding apparatus comprising decoding means for decoding a received coded image signal; and transformation means for altering the frame rate of the received coded image signal to be suitable for display according to the second frame rate.

Suitably, the image decoding apparatus further comprises any one or more of the features of the accompanying description, claims, abstract and/or drawings, in any combination.

The preferred embodiments of the present invention are described, by way of example only, with reference to the drawings wherein :

Figure 1 is a view showing a frame arrangement of one group-of-pictures (GOP) layer according to the international standard of the moving picture experts group (MPEG);

frame rate transformation function according to a preferred embodiment of the present invention;

Figure 3A is a view for explaining a frame rate transformation operation when a frame rate of an input bitstream is larger than that of an image display device;

Figure 3B is a view for explaining a frame rate transformation operation when a frame rate of an input bitstream is smaller than that of an image display device.

A preferred embodiment of the present invention will be described below in more detail with reference to Figures 1 through 3.

Figure 1 shows an image frame arrangement of one group-of-pictures (GOP) layer according to the international standard of the moving picture experts group (MPEG). The GOP is composed of three kinds of frames. An intra-coded (I) frame is image data coded using only intra-frame information, a predictive-coded (P) frame is data obtained by coding a moving vector and the differential data using movement predicted from a previous I frame or P frame, and bidirectionally-coded (B) frame is data obtained by coding a moving vector and the differential data using movement predicted from a previous and following I frame or P frame. As such, if an image is coded using interframe relevancy, a compression efficiency can be enhanced.

The present invention provides an apparatus which outputs a frame sequence to be coincident with a frame rate of an image display device when a frame rate of an input signal differs from that of the image display device.

Figure 2 is a block diagram of an image decoding apparatus having a frame rate transformation function according to a preferred embodiment of the present invention. In Figure 2, an input buffer 10 receives a coded image signal and outputs the same to a decoder 20. The decoder 20 decodes the input image signal, and stores the decoding result in a frame memory 30. The decoder 20 reads out the stored decoded image signal from the frame memory 30 and outputs the read data to an image display device via an image interfacer 40.

Meanwhile in the Figure 2 apparatus, a first frame rate generator 50 receives a reference clock signal and generates a frame rate of the input bitstream, that is, a first frame rate. A second frame rate generator 60 also receives the reference clock signal and generates a frame rate of the image display device, that is, a second frame rate. A frame rate transformer 70 receives the first and second frame rates respectively from the first and second frame rate generators 50 and 60, and generates a control signal for transforming the frame rate of the input bitstream into the frame rate of the image display device. The frame rate transformer 70 supplies the control signal to the decoder 20 which uses the same for controlling the output of the decoded image. In more detail, a first operation unit 73 in the frame rate transformer 70 receives the first and second frame rates respectively from the first and second frame rate generators 50 and 60, and calculates a threshold value for determining an omission or repetition point of time of a frame output from the decoder 20. A second operation unit 74 therein calculates a

delay time for delaying a predetermined frame of the input bitstream to be output as having a frame rate of the image display device. An omission determiner 71 receives the outputs of the first and second operation units 73 and 74 and determines a frame to be omitted among the decoded frames. Likewise, a repetition determiner 72 receives the outputs of the first and second operation units 73 and 74 and determines a frame to be repeated among the decoded frames.

The image interfacer 40 outputs the output of the decoder 20 to the image display device (not shown) according to the frame rate supplied from the second frame rate generator 60.

The operation of the Figure 2 apparatus having the above-described structure will be described below with reference to Figures 3A and 3B.

The input buffer 10 in the Figure 2 apparatus receives a bitstream of the compressively coded image signal and outputs the received image signal to the decoder 20. The decoder 20 performs a signal processing such as inverse quantization, inverse discrete cosine transform (IDCT) and motion compensation with respect to the input image signal from the input buffer 10, and decodes the received image signal into a prior-to-being compressively-coded image signal. The decoder 20 stores the decoded image signal in the frame memory 30.

The first frame rate generator 50 generates a frame rate of the input bitstream, that is, a first frame rate, based on a reference clock signal. The second frame rate generator 60 also generates a frame rate of the image display device, that is, a second frame rate, based on the reference clock

signal. The frame rate transformer 70 receives the first and second frame rates respectively from the first and second frame rate generators 50 and 60, and generates a control signal for controlling the output of the decoder 20 based on the difference between two frame rates.

The operational principle of outputting an input image signal of a first frame rate to an image display device of a second frame rate will be described with reference to Figure 3A.

A frame rate transformation operation in the case that a frame rate of an input bitstream is larger than that of an image display device is shown in Figure 3A. Figure 3A shows a case in which an input bitstream of the NTSC mode is input in a TV receiver having an image display device of the PAL mode.

As shown as (A) in Figure 3A, thirty frames per second are output in the NTSC mode. In other words, the interval of time of the output between the frames becomes 1/30 seconds. Meanwhile, the image display device of the PAL mode outputs twenty-five frames per second on a screen. That is, each frame is output every 1/25 seconds. Thus, if an input bitstream is output as the frame rate of the image display device, last five frames of the input bitstream are output too late corresponding to the difference between two modes, to thereby make a real-time image output impossible.

Here, a time length of outputting six frames of the input bitstream corresponds to that of the five frames in the image display device. Accordingly, if one frame is omitted every six frames in the frames of the

input bitstream, the input bitstream can be output meeting the frame rate of the image display device.

In more detail, as shown as (B) in Figure 3A, once the I frame being a start frame of the GOP layer is output, the following frames are output not meeting the 1/30 seconds being the frame rate of the input bitstream, but meeting the 1/25 seconds being the frame rate of the image display device. That is, the frames following the I frame are delayed by a predetermined time and then output to meet the frame rate of the image display device. Here, assuming that an initial delay time is Δ, the Δ corresponds to a difference (=1/25-1/30) between the interval of outputting the frame of the input bitstream and that of outputting the image in the image display device. In other words, the frames following the I frame have sequentially accumulated delay time such as 1Δ, 2Δ, 3Δ, ...

If the delay time is accumulated in this manner, the fifth frame of the input bitstream is displayed on the screen after 5Δ, that is, 1/30 seconds corresponding to the frame rate of the input bitstream elapsed from the displayed fourth frame. Thus, if the sixth frame of the input bitstream is omitted, the output point of time of the seventh frame thereof becomes coincident with the frame rate of the image display device. By repeating such an operation, the frame rate of the input bitstream can fit that of the image display device.

Here, it is desirable that a frame to be omitted is limited to a B frame including its own least frame information, to thereby minimize the deterioration of picture quality due to frame omission.

In Figure 2, the first operation unit 73 in the frame rate transformer 70 receives the first and second frame rates from the first and second frame rate generators 50 and 60, and calculates a threshold value for determining an omission point of time. The threshold value is for detecting when a delay time for outputting a predetermined frame of the input bitstream to have a frame rate of the image display device corresponds to an output interval 5Δ of the input bitstream. Accordingly, it is desirable that the threshold value is set to be somewhat smaller than the output interval 5Δ of the input bitstream. In the embodiment of the present invention, the first operation unit 73 calculates a time which is obtained by subtracting a reference delay time (Δ) divided by two from an output interval of the input bitstream, and outputs the calculation result to the omission determiner 71.

Meanwhile, the second operation unit 74 receives the first and second frame rates and calculates a reference delay time (Δ) corresponding to a difference between the two frame rates to calculate a delay quantity per each frame and outputs the calculated delay quantity to the omission determiner 71.

The omission determiner 71 compares the threshold value received from the first operation unit 73 and the delay quantity calculated in the second operation unit 74. By comparison, if the delay quantity is not less than the threshold value, the omission determiner 71 judges whether the corresponding frame is a B frame. When it is judged that the delay quantity is not less than the threshold value and the corresponding frame is a B frame, the omission determiner 71 generates an omission control signal.

The decoder 20 outputs the image signal stored in the frame memory 30 to the image interfacer 40. The decoder 20 omits a frame having a turn

to be output to the image interfacer 40 when an omission control signal is input from the omission determiner 71, and outputs the following frames to the image interfacer 40.

The image interfacer 40 outputs the decoded image output from the decoder 20 to the image display device, according to the frame rate generated from the frame rate generator 60.

An operation of the case in which the frame rate of the input bitstream is smaller than the frame rate of the image display device, is shown in Figure 3B. Figure 3B shows an example of the case in which a TV receiver having an image display device of the NTSC mode receives an input bitstream of the PAL mode. Through a reverse process to Figure 3A, the frame rate can be transformed. That is, as shown in Figure 3B, the output time of the five frames of the input bitstream corresponds to the output time of the six frames in the image display device. Thus, if the frame of the input bitstream repeats every five frame, the input bitstream can be output coincident with the frame rate of the image display device. Here, the input bitstream should be output a predetermined time earlier than the frame output interval of the input bitstream, so that the input bitstream is output to have the frame rate of the image display device. The time-leading reference time uses the same Δ as that of the above-described reference delay time.

The repetition determiner 72 compares the threshold value input from the first operation unit 73 and the delay quantity calculated in the second operation unit 74. Here, the delay quantity becomes a negative value, that is, a reduced quantity. By comparison, if the reduced quantity is not less than the threshold value, the repetition determiner 72 generates a repetition control

signal. The decoder 20 outputs a previously output frame to the image interfacer 40 once more, when a repetition control signal is received from the repetition determiner 72.

As described above, the decoding apparatus according to the present invention transforms an image signal having a frame rate different from that of an image display device into one having the frame rate of the image display device. As a result, an image having a frame rate different from that of the image display device can be displayed via the same image display device.

While only certain embodiments of the invention have been specifically described herein, it will be apparent that numerous modifications may be made thereto without departing from the spirit and scope of the invention.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative

features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. An image decoding apparatus which transforms a coded image signal having a frame rate different from that of an image display device to have the frame rate of the image display apparatus and outputs the transformed image signal, the image decoding apparatus comprising :

decoding means for decoding the received coded image signal;

first frame rate generation means for generating a first frame rate of the coded image signal based on a predetermined reference clock signal;

second frame rate generation means for generating a second frame rate of an image display device based on the reference clock signal;

frame rate transformation means for receiving the first and second frame rates respectively generated from said first and second frame rate generation means, and generating an omission control signal for omitting a predetermined frame when the first frame rate is larger than the second frame rate, while generating a repetition control signal for repeating a predetermined frame when the first frame rate is smaller than the second frame rate; and

image interfacing means for outputting a frame sequence output from said decoding means to meet the frame rate of said image display device.

2. An image decoding apparatus according to claim 1, wherein said frame rate transformation means generates an omission or repetition control signal based on a delay time for outputting a predetermined frame of the input bitstream to have the frame rate of said image display device.

3. An image decoding apparatus according to claim 2, wherein said frame rate transformation means generates an omission control signal when said delay time is not less than a predetermined threshold value.

4. An image decoding apparatus according to claim 2, wherein said frame rate transformation means generates an omission control signal when said delay time is not less than the predetermined threshold value and the corresponding frame is a bidirectionally-coded (B) frame.

5. An image decoding apparatus according to claim 2, wherein said frame rate transformation means generates a repetition control signal when a sign of said delay time is negative and an absolute value of said delay time is not less than a predetermined threshold value.

6. An image decoding apparatus according to claim 3 or claim 4, wherein said threshold value is set to be somewhat smaller than the frame rate of the input bitstream.

7. An image decoding apparatus according to claim 5, wherein said threshold value is set to be somewhat smaller than the frame rate of the input bitstream.

8. An image decoding apparatus according to any preceding claim, wherein said frame rate transformation means comprises :

a first operation unit for calculating a predetermined threshold value;

a second operation unit for calculating a time delayed for outputting the input signal to have the frame rate of said image display device;

an omission determiner for receiving the threshold value and the delay time and generating an omission control signal when a sign of the delay time is positive and an absolute value thereof is larger than the threshold value; and

a repetition determiner for receiving the threshold value and the delay time and generating a repetition control signal when a sign of the delay time is negative and an absolute value is larger than the threshold value.

9. An image decoding apparatus for transforming a coded image signal having a first frame rate to a signal suitable for display on an image display apparatus operating at a second frame rate, the image decoding apparatus comprising decoding means for decoding a received coded image signal; and transformation means for altering the frame rate of the received coded image signal to be suitable for display according to the second frame rate.

10. An image decoding apparatus according to claim 9, further comprising any one or more of the features of the accompanying description, claims, abstract and/or drawings, in any combination.

11. An image decoding apparatus, substantially as described herein, with reference to and as shown in Figure 2 of the accompanying drawings.

The Patent Office

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Application No: GB 9619949.2 **Examiner:** John Donaldson
Claims searched: 1 to 11 **Date of search:** 12 November 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4F(FEP, FEX, FKE)

Int Cl (Ed.6): H04N 5/00, 5/44, 5/46, 7/00, 7/01

Other: Online:WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2154825 A	(SONY), see page 3, lines 13 to 62	1 to 3, 5 to 10
X	GB 2016858 A	(SONY), see page 1, lines 66 to 80, page 1, line 94 to page 2, line 11, page 3, lines 115 to 119	1 to 3, 5 to 10
X	GB 1306130	(NIPPON), see page 3, line 123 to page 4, line 3, page 4, lines 76 to 85, page 5, lines 52 to 77, page 7, lines 71 to 86	1 to 3, 5 to 10
X	GB 1270552	(NIPPON), see page 15, lines 19 to 40, page 19, lines 24 to 27, page 19, lines 89 to 104	1 to 3, 5 to 10
X	US 5453792	(GIFFORD), see column 5, lines 5 to 38	1 to 3, 5 to 10

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